CLAIMS

1. A lateral semiconductor device, the device comprising a semiconductor layer on an insulating substrate, the semiconductor layer having a first region of a first conduction type and a second region of a second conduction type with a drift region therebetween, the drift region being provided by a third region of the first conduction type and a fourth region of the second conduction type, the third and fourth (drift) regions being so arranged that when a reverse voltage bias is applied across the first and second regions of the semiconductor layer, the third region has locally in the proximity of the first region an excess of impurity charge relative to the fourth region, and the fourth region has locally in the proximity of the second region an excess of impurity charge relative to the third region, and the total volume charge in the third region is substantially equal to the total volume charge in the fourth region.

2. A lateral semiconductor device, the device comprising a semiconductor layer on an insulating substrate, the semiconductor layer having a first region of a first conduction type and a second region of a second conduction type with a drift region therebetween, the drift region being provided by a third region of the first conduction type and a fourth region of the second conduction type, the third and fourth (drift) regions being so arranged that when a reverse voltage bias is applied across the first and second regions of the semiconductor layer, the impurity charge in the third region varies with a positive slope along the device from the first region to the second region and the charge in the fourth region varies with a negative

slope along the device from the first region to the second region and such that the total charge in the volume of the third region is substantially equal to the total charge in the volume of the fourth region.

3. A device according to claim 2, wherein the impurity charge in the third region varies substantially linearly with a positive slope along the device from the first region to the second region.

4. A device according to claim 2, wherein the impurity charge in the fourth region varies substantially linearly with a negative slope along the device from the first region to the second region.

5. A device according to claim 1, wherein only part of the drift region is placed above an insulating substrate, the rest of the substrate comprising at least a region of semiconductor material.

6. A device according to claim 1, wherein the largest part of the drift region is placed above an insulating substrate such that the high voltage end of the drift region has no semiconductor layer underneath and the low voltage end of the drift region is positioned over a substrate that contains at least a region of semiconductor material.

7. A device according to claim 1, wherein the third (drift) region is continuous along the device from the first region to the second region.

8. A device according to claim 1, wherein the fourth (drift) region is continuous along the device from the first region to the second region.

9. A device according to claim 1, wherein the third (drift) region is provided by or includes a plurality of semiconductor islands in the fourth (drift) region.

10. A device according to claim 9, wherein the islands are electrically floating.

11. A device according to claim 1, wherein the fourth (drift) region is provided by or includes a plurality of semiconductor islands in the third (drift) region.

12. A device according to claim 11, wherein the islands are electrically floating.

13. A device according to claim 1, wherein the third (drift) region includes or is provided by a plurality of semiconductor islands in a common silicon background layer having lower doping than any of the third (drift) regions.

14. A device according to claim 1, wherein the fourth (drift) region includes or is provided by a plurality of semiconductor islands in a common silicon background layer having lower doping than any of the fourth (drift) regions.

15. A device according to claim 13, wherein the background layer has the same conductivity type as the islands such that said islands are electrically connected to each other by the background layer.

16. A device according to claim 1, wherein the charge variation in the third and fourth regions is a function of the permittivity of the insulating substrate such that the higher the dielectric permittivity of the insulating substrate the higher the slope of the charge variation in the third and fourth drift regions.

17. A device according to claim 1, wherein the charge variation in the third and fourth regions along the device structure from the first region to the second region is achieved by varying the in-plane area of these regions.

18. A device according to claim 1, wherein the charge variation in the third and fourth regions along the device structure from the first region to the second region is achieved by varying the impurity doping concentration of these regions.

19. A device according to claim 18, wherein the doping concentration in the third region varies with a positive slope from the first region to the second region while the doping concentration in the third region varies with a negative slope from the first region to the second region such that the average doping concentration in the third region along the device structure from the first to the second region is substantially equal to the average doping concentration in the fourth region along the device structure from the first to the second region.

20. A device according to claim 19, wherein the slope of the doping concentration variation is proportional to the dielectric permittivity of the substrate.

21. A device according to claim 1, wherein the third and the fourth regions are placed adjacent to each other in the third dimension.

22. A device according to claim 1, wherein the third and fourth regions are placed above each other.

23. A device according to claim 1, wherein the semiconductor layer comprises at least one of silicon, silicon-carbide, gallium-arsenide, gallium-nitride and III-V semiconducting materials.

24. A device according to claim 1, wherein the insulating (dielectric) layer comprises at least one of air, sapphire, diamond, aluminium-nitride, silicon dioxide, silicon-nitride, any mould material used for IC packages, and passivation dielectric material known in microelectronics.

25. A device according to claim 2, wherein only part of the drift region is placed above an insulating substrate, the rest of the substrate comprising at least a region of semiconductor material.

26. A device according to claim 2, wherein the largest part of the drift region is placed above an insulating substrate such that the high voltage end of the drift region has no semiconductor layer underneath and the low voltage end of the drift region is positioned over a substrate that contains at least a region of semiconductor material.

27. A device according to claim 2, wherein the third (drift) region is continuous along the device from the first region to the second region.

28. A device according to claim 2, wherein the fourth (drift) region is continuous along the device from the first region to the second region.

29. A device according to claim 2, wherein the third (drift) region is provided by or includes a plurality of semiconductor islands in the fourth (drift) region.

30. A device according to claim 29, wherein the islands are electrically floating.

31. A device according to claim 2, wherein the fourth (drift) region is provided by or includes a plurality of semiconductor islands in the third (drift) region.

32. A device according to claim 31, wherein the islands are electrically floating.

33. A device according to claim 2, wherein the third (drift) region includes or is provided by a plurality of semiconductor islands in a common silicon background layer having lower doping than any of the third (drift) regions.

34. A device according to claim 2, wherein the fourth (drift) region includes or is provided by a plurality of semiconductor islands in a common silicon background layer having lower doping than any of the fourth (drift) regions.

35. A device according to claim 33, wherein the background layer has the same conductivity type as the islands such that said islands are electrically connected to each other by the background layer.

36. A device according to claim 2, wherein the charge variation in the third and fourth regions is a function of the permittivity of the insulating substrate such that the higher the dielectric permittivity of the insulating substrate the higher the slope of the charge variation in the third and fourth drift regions.

37. A device according to claim 2, wherein the charge variation in the third and fourth regions along the device structure from the first region to the second region is achieved by varying the in-plane area of these regions.

38. A device according to claim 2, wherein the charge variation in the third and fourth regions along the device structure from the first region to the second region is achieved by varying the impurity doping concentration of these regions.

39. A device according to claim 38, wherein the doping concentration in the third region varies with a positive slope from the first region to the second region while the doping concentration in the third region varies with a negative slope from the first region to the second region such that the average doping concentration in the third region along the device structure from the first to the second region is substantially equal to the average doping concentration in the fourth region along the device structure from the first to the second region.

40. A device according to claim 39, wherein the slope of the doping concentration variation is proportional to the dielectric permittivity of the substrate.

41. A device according to claim 2, wherein the third and the fourth regions are placed adjacent to each other in the third dimension.

42. A device according to claim 2, wherein the third and fourth regions are placed above each other.

43. A device according to claim 2, wherein the semiconductor layer comprises at least one of silicon, silicon-carbide, gallium-arsenide, gallium-nitride and III-V semiconducting materials.

44. A device according to claim 2, wherein the insulating (dielectric) layer comprises at least one of air, sapphire, diamond, aluminium-nitride, silicon dioxide, silicon-nitride, any mould material used for IC packages, and passivation dielectric material known in microelectronics.